Electronic Version

Stylesheet Version v1.1.1

METHOD FOR REDUCED ELECTRICAL FUSING TIME

Abstract

A method and electrical fuse circuit design for reducing the testing time for a semiconductor device manufactured with redundant eFuse circuitry. A two-to-one multiplexer (MUX) is provided at each eFuse circuit in addition to the fuse latch and pattern latch and other logic components the eFuse circuit. Information on which fuse is to be blown is stored in the fuse's pattern latch. The output generated by the pattern latch is ANDed with a program input to provide a select signal for the MUX. Based on the select signal, the MUX allows the shifted "1" to either go to the next latch in the shift chain or bypass the next latch or latches in the shift chain depending on whether the next fuse is to be blown. Accordingly, rather than serially shifting through each fuse latch within the device, the invention enables only those fuse latches associated with fuses that are to be blown to hold up the propagation of the shifted "1" to the next eFuse circuits.